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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/740,469	12/22/2003	Kouichi Takagi	118153	3615
25944	7590	08/23/2006	EXAMINER	
OLIFF & BERRIDGE, PLC P.O. BOX 19928 ALEXANDRIA, VA 22320			NGUYEN, HOA CAO	
			ART UNIT	PAPER NUMBER
			2841	

DATE MAILED: 08/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/740,469	TAKAGI ET AL.
	Examiner Hoa C. Nguyen	Art Unit 2841

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 05 June 2006.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-6 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-6 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. The amendment filed on 6/5/06 has been entered. Applicants have amended the drawings and claims 1 and 2. Claim 7 is cancelled.

Drawings

2. The amended drawing(s) is/are approved. The objection(s) to the drawing(s) is/are withdrawn.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-6 are rejected under 35 U.S.C. 103(b) as being anticipated by Kawakita et al. (US 20040001319) in view of Okada et al. (US 6534726).

Regarding claim 1, as shown in figures 1, 4 and 6, Kawakita et al. disclose a control circuit board 20 (paragraph 34) comprising:

(a) A plurality of bus bars 10 (a bus bar group, paragraph 28) that are bonded to a surface of the control circuit board 20 (paragraph 34) in a state that the bus bars 10 are arranged approximately in the same plane (also see paragraph 38); and

(b) connection terminals 12/14/16 (paragraph 30) for connecting to an external circuit and fuses (it is noted that bus bars 12/14/16 are extended outward toward the end portions or the side edges of the control circuit board 20).

But, Kawakita et al. fail to disclose a connecting portion to be connected to an external circuit, wherein the connecting portion is configured such that an end portion of the control circuit board is formed with a cut which is opened sideways and is coated with a general semi-circular conductor layer in such a manner that an inner side surface of the cut is covered with the conductor layer, an inner circumferential surface of the conductor layer is connected to a circuit that is incorporated in the control circuit board.

Okada et al., as shown in figures 3-4 and 8, disclose a circuit board 11 (a module substrate) having electronic components and circuit patterns formed thereon (figures 1 and 8, col.7:1-12 and col.2:18-28). The circuit board 11 has a connecting portion 13 (end-face through-hole) for connecting to a circuit element formed on another circuit board (a mother board) by solder 17/18 (solder/fillet, col.7:34-48). The connecting portion 13 is configured such that an end portion of the board 11 is formed with a cut 14 (an end-face opening groove, col.7:13-18) which is opened sideways and is coated with a general semi-circular conductor layer 15 (end-face electrode) in such a manner that an inner side surface of the cut 14 is covered with the conductor layer 15, an inner circumferential surface of the conductor layer (clearly shown in figures 3-4) is connected to a circuit 16 (wiring, the circuit formed on the board 11, col.7:27-33) that is incorporated in the circuit board 11.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the teachings about the connecting portion 13 of Okada et al. on the control circuit board 20 of Kawakita et al. at least at the side edges where the bus bars 12/14/16 are bended in order to surely bond the bus bars layer onto the control circuit board 20 even if the board or the bus bars layer is warped and to prevent the bus bars 12/14/16 from bending/loosing away from the board 20 when force is applied by a plug-in connector.

Thus, the teaching(s) from Okada on the board of Kawakita provides a connecting portion (the end face through-hole 13) to be connected to the bus bars 12/14/16, wherein the connecting portion is configured such that an end portion of the board 20 is formed with a cut 14 (taught by Okawa) which is opened sideways and is coated with a general semi-circular conductor layer 15 (taught by Okawa) in such a manner that an inner side surface of the cut is covered with the conductor layer 15 (taught by Okawa), an inner circumferential surface of the conductor layer is connected to a circuit that is incorporated in the circuit board 20 (the control circuit formed on the board 20).

Examiner remarks: It is noted that the teachings from Okada is centering about an edge connection portion of a substrate that are not limited to a connection between a substrate to a pad formed on another board. Therefore, it is understood that the teachings is not limited to a pad itself but also to any conductive layer.

Regarding claim 2, Kawakita et al. (as shown in figures 1, 4 and 6) in view of Okada et al. (as shown in figures 3-4 and 8) disclose every limitation as shown in claim 1 above including a circuit structural body comprising:

- (a) A plurality of bus bars 10 that are part of a power circuit (no number, see abstract or paragraph 2),
- (b) the power circuit (formed on substrate 20) are bonded to a surface of a control circuit board 20 in a state that the bus bars 10 are arranged approximately in the same plane,
- (c) the control circuit board 20 including a connecting portion 13 (the teaching from Okada, discussed in claim 1 above) to be connected to an external circuit, the connecting portion is configured such that an end portion of the control circuit board is formed with a cut 14 which is opened sideways and is coated with a generally semi-circular conductor layer 15 in such a manner that an inner side surface of the cut 14 is covered with the conductor layer 15, the conductor layer 15 is connected to a circuit that is incorporated in the control circuit board 20,
- (d) wherein a particular one of the bus bars 10 (section of terminal 12/14/16) is electrically connected to the circuit incorporated in the control circuit board 20 by soldering 17 (formed into fillet 18, col.7:34-48, the teaching from Okada) in which solder 17 is supplied so as to bridge an inner circumferential surface of the conductor layer 15 of the control circuit board and a surface of the particular one of the bus bar 10 in a state that a coating portion of the conductor layer is laid on the particular bus bar.

Regarding claim 3, as clearly shown in figure 4, Kawakita et al. in view of Okada et al. disclose every limitation as shown in claim 2 above including a switching element 30 (a relay switch, paragraph 35), which is provided in the power circuit including the bus bars 10, the control circuit board 20 incorporates a control circuit for controlling driving of the switching element 30, and the switching element 30 is mounted so as to bridge the bus bar 10 and the control circuit board 20.

Regarding claim 4, as clearly shown in figure 1, Kawakita et al. in view of Okada et al. disclose every limitation as shown in claim 2 above including a plurality of bus bars 10 (section of terminal 12/14/16) project sideways from the control circuit board 20 to serve as terminals to be connected to the external circuit, and at least part of the bus bars (at the side edge of the board 20) to serve as the terminals that are electrically connected to the conductor layers 15 by soldering 17.

Regarding claim 5, as clearly shown in figure 1, Kawakita et al. in view of Okada et al. disclose every limitation as shown in claims 2 and 4 above including the bus bars 10 to serve as the terminals (12/14/16) that are bent in the same direction (a section of the terminal is bent upward) that is generally perpendicular to the control circuit board 20.

Regarding claim 6, as shown in figure 1, Kawakita et al. in view of Okada et al. disclose every limitation as shown in claims 2 and 4 above including the terminals 12/16 that include signal input terminals 12 to which instruction signals are input externally, and the bus bars to serve as the signal input terminals are electrically connected to the conductor layers 15 (the teaching from Okada).

Response to Arguments

5. Applicant's arguments with respect to claims 1-6 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

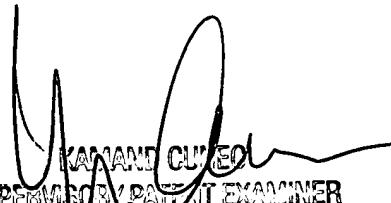
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hoa C. Nguyen
2/28/06



KAMAND CUEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800